We claim:

1. A microelectronic apparatus having protection against high frequency crosstalk radiation, comprising:

a planar insulating substrate;

an active semiconductor electronic device located over a first region of said insulating substrate; and

a doped semiconductor located in a second region of said insulating substrate substantially surrounding said first region.

2. The microelectronic apparatus of claim 1, in which said doped semiconductor is routed to ground.

3. The microelectronic apparatus of claim 1, in which said doped semiconductor fills a trench located in said second region.

4. The microelectronic apparatus of claim 1, further comprising a dissipative conductor overlaying and adjacent to said doped semiconductor.

5. The microelectronic apparatus of claim 1, further comprising:

a second active semiconductor electronic device located over a third region of said insulating substrate, said third region being substantially separated from said first region by said second region.

6. The microelectronic apparatus of claim 1, in which said doped semiconductor comprises an n type semiconductor dopant.

7. The microelectronic apparatus of claim 4, further comprising:

a dielectric passivation layer having a first surface overlaying said insulating substrate and having a second surface;

said dielectric passivation layer having a thickness extending between said first and second surfaces;

said dissipative conductor extending into said dielectric passivation layer.

8. The microelectronic apparatus of claim 4, in which the dissipative conductor is a metal.

9. The microelectronic apparatus of claim 5, in which said first and second active semiconductor electronic devices are selected from the group consisting of transistors, circuits, integrated circuits, diodes, and memory cells.

10. The microelectronic apparatus of claim 7, in which said dissipative conductor fills a trench located in said dielectric passivation layer.

11. The microelectronic apparatus of claim 7, in which said dissipative conductor extends from said first surface toward said second surface over at least about half of said thickness.

12. The microelectronic apparatus of claim 7, further comprising:

metallic test probe contacts located at said second surface, said metallic test probe contacts making electrical connections with said active semiconductor electronic device.

13. The microelectronic apparatus of claim 11, in which said dissipative conductor extends from said first surface to said second surface.

14. A method of making a microelectronic apparatus having protection against high frequency crosstalk radiation, comprising the steps of:

providing a planar insulating substrate;

forming an active semiconductor electronic device located over a first region of said insulating substrate; and

forming a doped semiconductor located in a second region of said insulating substrate substantially surrounding said first region.

15. The method of claim 14, in which said doped semiconductor is formed by the step of implanting dopant ions in a trench located in said second region.

16. The method of claim 14, further comprising the step of forming a dissipative conductor overlaying and adjacent to said doped semiconductor.

17. The method of claim 14, further comprising the step of forming a second active semiconductor electronic device located over a third region of said insulating substrate, said third region being substantially separated from said first region by said second region.

18. The method of claim 16, further comprising the step of:

forming a dielectric passivation layer having a first surface overlaying said insulating substrate and having a second surface;

said dielectric passivation layer having a thickness extending between said first and second surfaces;

said dissipative conductor extending into said dielectric passivation layer.

19. The method of claim 18, in which said dissipative conductor is formed by the steps of:

providing a trench located in said dielectric passivation layer; and

filling a dissipative conductor into said trench.

20. The method of claim 18, further comprising the step of:

forming metallic test probe contacts located at said second surface, said metallic test probe contacts making electrical connections with said active semiconductor electronic device.